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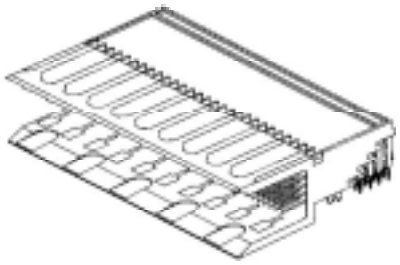
PHENIX
Time Expansion Chamber
Preamp-Shaper Electronics and Interfacing specifications

I. Interface to the TEC Anode Board:

- Interface between the TEC-PS and the TEC Anode Board using AMP Z-PACK[i] 2mm Future Bus connectors.



- Four 24 Pin connectors per TEC-PS board
- Male Z-PACK connectors on the TEC-PS board.
- Connectors are mounted on the Bottom[ii] side of the printed circuit board.

- External ESD protection on the Input lines for the TEC-PS Integrated circuits.

II. Power and Ground:

- Unregulated Power Supply feed from the Anode boards, through the Z-PACK connectors. The following unregulated supplies are required from the Anode board for local regulation.

    1. +3.0 Volts [minimum] for +2.5 Volts regulation.
    2. +6.0 Volts [minimum] for +5.0 Volts regulation.
    3. -6.0 Volts [minimum] for -5.0 Volts and -2.5 Volts regulation.
    4. 0 Volts, Power Supply Ground and Preamp/Shaper Return.

- Power supply for the TEC-PS board electronic components are regulated locally on every board. The following regulated voltages are available on the TEC-PS board along with Ground.

    1. +2.5 Volts.
    2. -2.5 Volts.
    3. +5.0 Volts.
    4. -5.0 Volts.

- Power Consumption[iii] per TEC-Preamp-Shaper board.[Quiescent current]

    1. +3.0 Volts: 400mA [1.2 Watts]
    2. +6.0 Volts: 220mA [1.32 Watts]
    3. -6.0 Volts: 550mA [3.3 Watts]

    - Total Power consumption: 5.82 Watts/32 channels.

- TEC-PS Preamp returns are ganged together to the ground plane of the Printed circuit board.

III. Geographical Addressing for TEC-PS Boards:

- Geographical Addressing from each PS board on every TEC plane:

  - 15 boards/plane requiring 4 ID bits.
  - ID bits are routed into the PS board through the Anode Interface Z-PACK connectors.
  - Logic Levels of ID bits from the Anode Board: +3.0 Volts : "ONE"
    0 Volts : "ZERO"
  - ID bits are level translated into RS-422 Signals and shipped to the FEM through the output connectors.

IV. Mechanical specifications of the TEC-PS Board:

- Mechanical Dimension and Board Clearances of the TEC-PS board.

Board width	: 3.75"	maximum
Board Edge to Component clearance	: 0.1875"	minimum
Board Thickness	: 0.0625"	maximum
Board Length	: ***Layout imposed***	
Component height on the Solder side	: 0.236"	maximum
Component height on the component side	: 1.00"	maximum

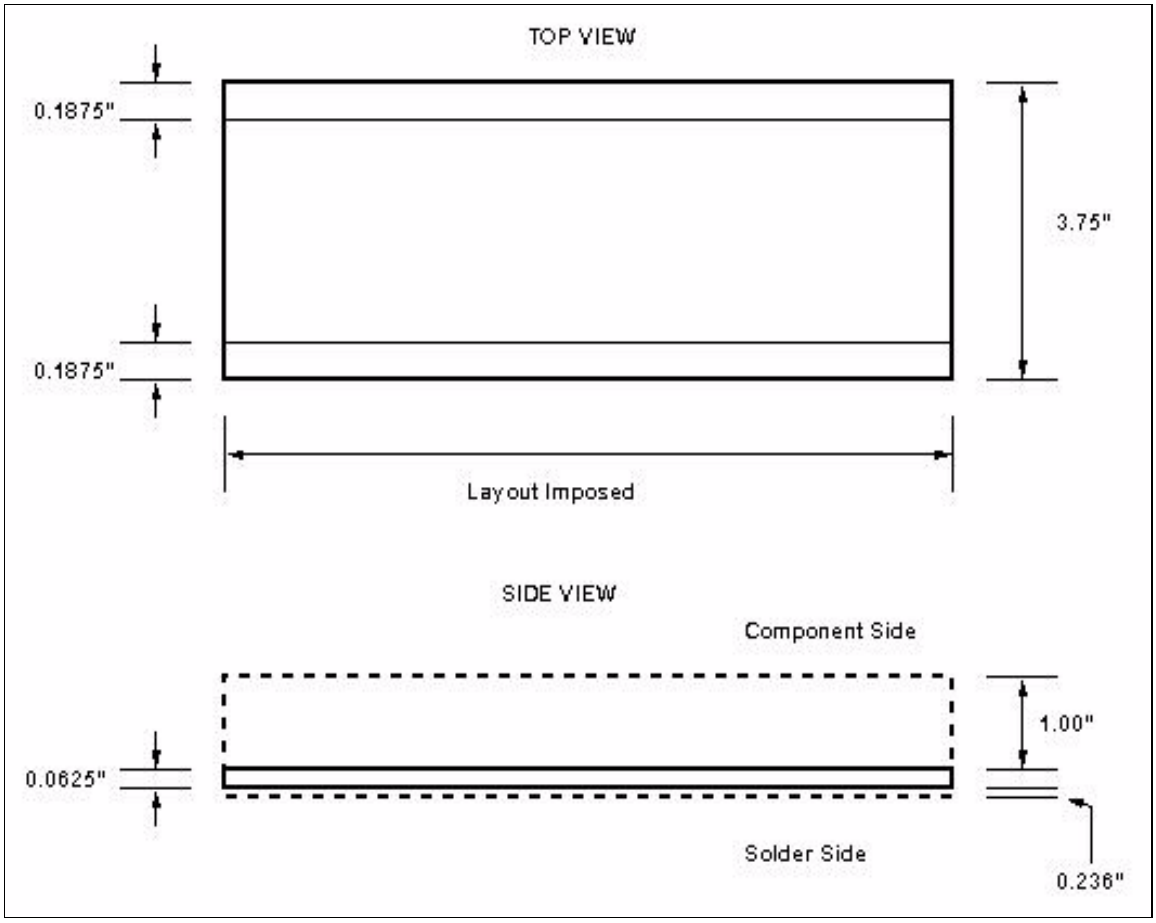


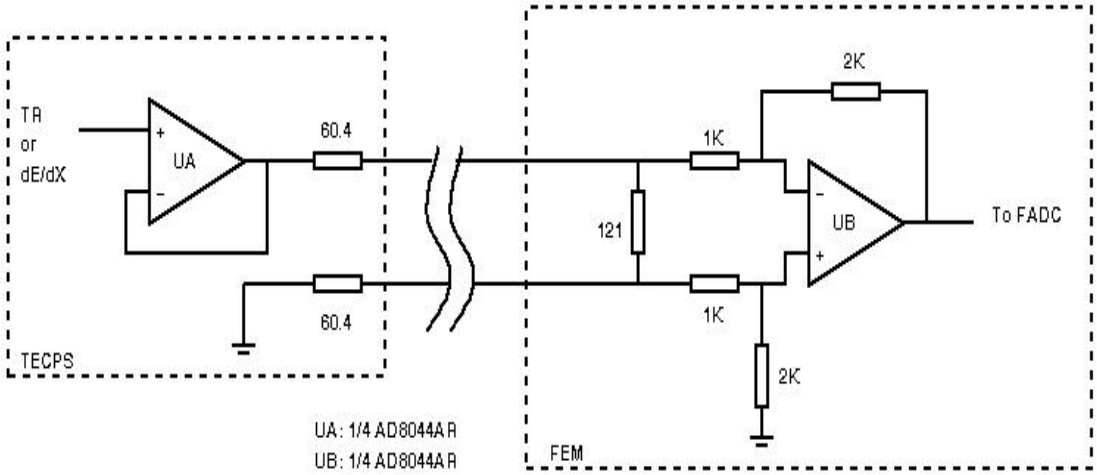
Figure 1

V. Interface to the FEM Board:

a. Preamp-Shaper:

- 32 Preamp-Shaper Channels per TEC PS board.
    1. 32 dE/dX outputs.
    2. 32 TR outputs.

- Pseudo Differential output Line drivers for TR and dE/dX signals to the FEM.



- TEC-PS to TEC-FEM interface using Amphenol 0.025" Twist 'N' Flat planar cable[iv], 40 twisted pairs.
- Amphenol 0.025" High-Density connectors for output cable interface.
    - Amphenol's Cable mount High density IDC sockets[v].
    - Amphenol's Board mounted High density straight IDC headers[vi].
- Output connectors are mounted on the bottom[vii] side of the TEC-PS board and should be within the maximum clearance allowed (1.00").

b. Control, Calibration, Read-back and Monitoring:

- TEC-PS configuration [Gain, Calibration mask and Channel Mask] are set using serial stream downloaded from the FEM.
    - All control lines given below are fully differential using RS-422 protocol.
        1. Serial Data Input.
        2. Serial Clock.
        3. Serial Data Load.
        4. Serial Data Output [Read-back].

- Onboard Calibration circuit.
    - On Board DAC and switching circuitry for Preamp/Shaper Calibration.
    - Maximum Calibration charge : 200fC.
    - Calibration Strobe signal from the FEM as differential RS-422 signal.
    - DAC programmed from the FEM using the same serial stream used for configuring the TEC-PS Integrated circuits.

- Onboard PLD is used for converting part of the serial stream [12 bits] to parallel data for the DAC. The PLD is a feed through for the entire serial stream which consists of data to configure 4 TEC-PS integrated circuits.

- No ground connection to exist between the FEM and the TEC-PS boards. All control and data signal [Calibration strobe, Serial and Analog] are differential, Analog signal output to the FEM are pseudo differential. The serial link, calibration strobe and address bits are fully differential using RS-422 protocol.

- Two 40 pair cables for output and control signals to and from the FEM and TEC-PS board.
    - ♦ dE/dX and TR signals interleaved on two output connectors.

- Input connector for pulsing the TEC-PS integrated circuits for diagnostics purposes, circumventing the onboard calibration circuitry. [A 2 pin SIP header is sufficient].

- Input connector for diagnosing the serial link. [This connector is separate from the output connector].
    - ♦ This diagnostic serial link has to be RS-422 signals.

VI. Serial Link Specifications:

- Data is latched into the shift register flip-flops on the falling edge of the clock.
- Total number of bits per TEC-Preamp-Shaper Integrated circuit:

1. Control:				
	♦ Peaking Time	:	2	bits
	♦ Tail Cancellation	:	3	bits
	♦ Gain	:	3	bits
2. Calibration		:	8	bits
3. Channel Mask		:	8	bits
	Total	:	24	bits

- Total number of bits per TEC-Preamp Shaper Board:

♦ DAC		:	12	bits
♦ TEC-PS	(4 x 24 bits)	:	96	bits
	Total	:	108	bits

- Serial Protocol:

    1. The entire serial stream (108 bits) are shifted in, on the negative edge of the serial clock.
    2. A falling edge on the LOAD line latches the serially shifted data onto the configuration registers of the TEC-PS integrated circuits and the output bits of the PLD for the DAC.
    3. The data-out of each chip in the chain is delayed by ½ a clock cycle to eliminate any flip-flop setup violations.

- The entire Serial stream for the TEC-PS board is as shown in Figure 2:

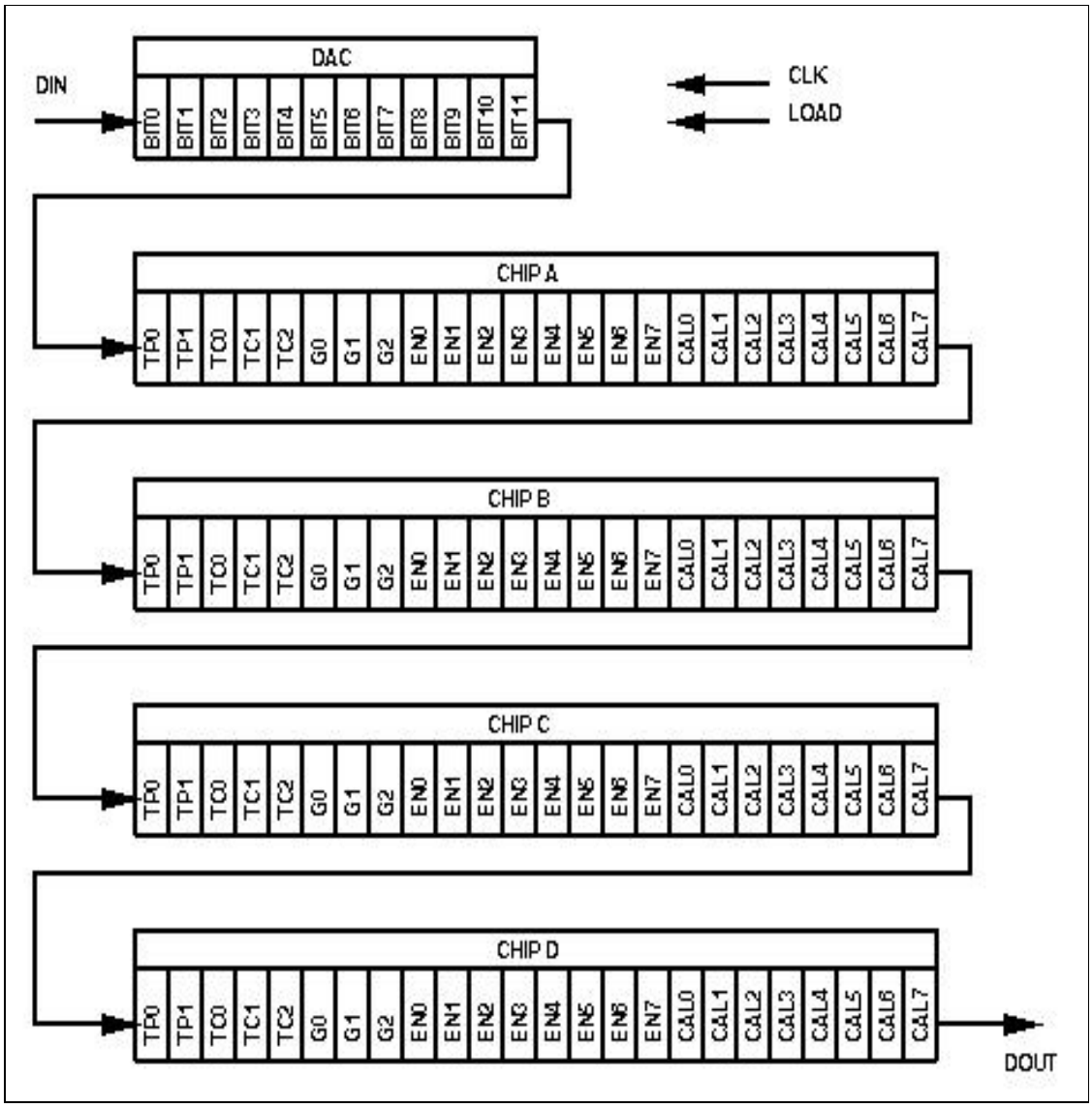


Figure 2

VII. Thermal Management:

- The Packages chosen for the Local Power regulators does not impose the need for any additional heat sinks for the regulators for any power dissipation considerations and thermal runaway of the regulators.

- Overall Thermal management method for the TEC-PS board has to be discussed and finalized.

IX. TEC-PS Printed Circuit Board Assembly and Connector details:

- All components with the exception of capacitors and resistors can be mounted on the bottom side [Solder side].

- Input Connector Pin count:

1.	Anode wire inputs	:	32	
2.	Ground [Preamp Returns + Power Ground]	:	48	
3.	Power +3.0 Volts	:	3	
4.	Power +6.0 Volts	:	3	
5.	Power -6.0 Volts	:	6	
6.	ID Bits [Geographical Addressing Bits]	:	4	
	Total Used	:	96	
	Used/Total	:	96/96	[100% Utilized]

- Output Connector Pin count [in pairs]:

1.	dE/dX outputs	:	32	
2.	TR outputs	:	32	
3.	Serial Download	:	3	
4.	Serial Read back	:	1	
5.	Calibration Strobe	:	1	
6.	ID Bits [Geographical Addressing Bits]	:	4	
	Total Used	:	73	
	Used/Total	:	73/80	[91.2% Utilized]

a. Input Connector Pin assignment scheme for the TEC-PS board:

The TEC-PS board is designed the right side up and its inverted and interfaced to the TEC anode boards. This requires extensive mapping of the pins from the Anode board to the TEC-PS board. The figure and the pin numbers give below are for the right side up [Good only for layout needs and Test bench]. Only on inverting and interfacing it to the anode boards, the pins and the signal correspond to the correct mapping.

Figure 3 shown below is the 4 Z-PACK connectors on the TEC-PS board along with the naming scheme followed:

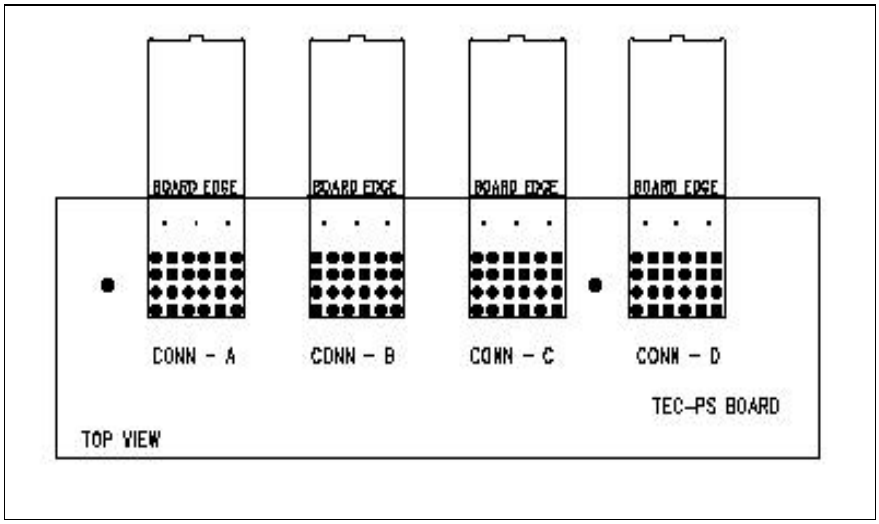


Figure 3

The TEC-PS board layout is approached in the following manner, since the TEC-PS board has to be interfaced to the TEC-Anode board inverted. Since the CAD software's work on the top-down topology, the board is designed as a 180 degree flipped. The scheme is illustrated in figure 4 and 5.

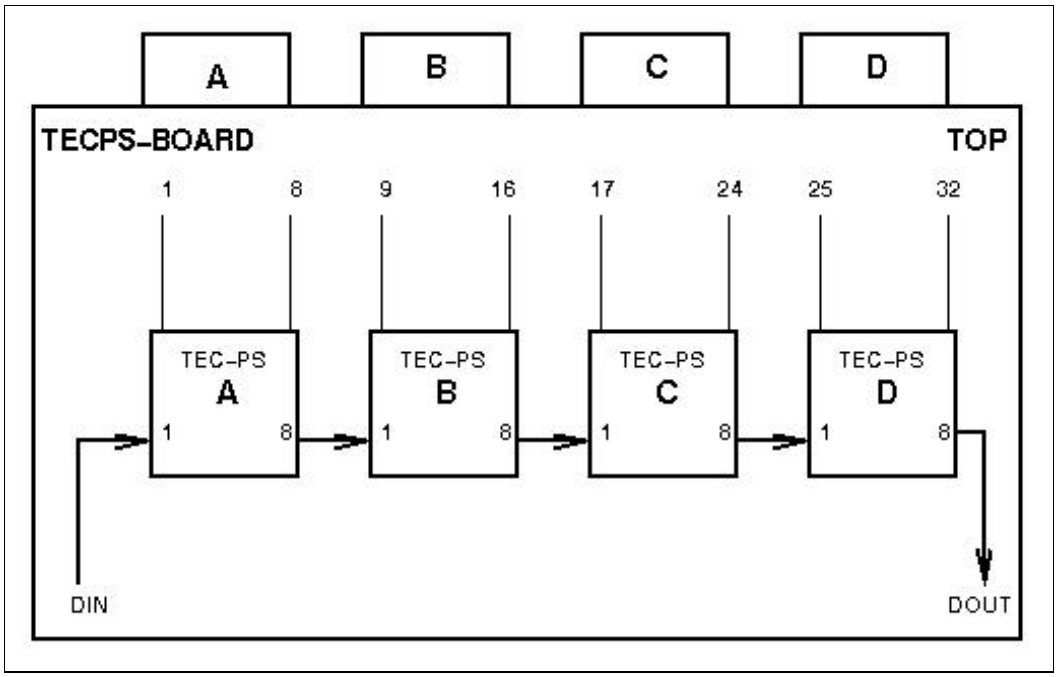


Figure 4

Figure 4 illustrates how the layout designer and the test bench engineer interprets the TEC-PS board. The channels are number from Left to right as Anode 0 to Anode 31. Note only partial modules are shown in these figures. This figure is the only figure of use for pin assignment for layout of the TEC-PS board.

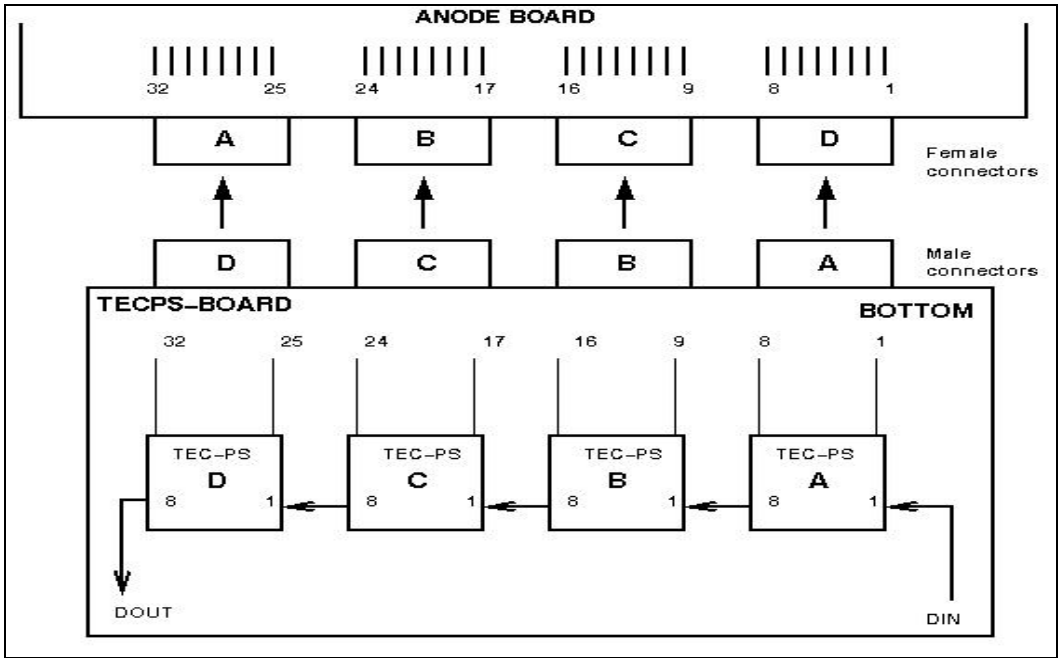


Figure 5

Figure 5 depicts how the TEC-PS board will be flipped and interfaced to the TEC Anode board. This figure is looking through the TEC-PS printed circuit board and the components are on the bottom side.

Input connector pin assignment:

- Anode signal assignments:

Anode	CHIP	Connector	Pin Number
0	A	B	2
1	A	B	4
2	A	B	5
3	A	B	7
4	A	B	10
5	A	B	12
6	A	B	13
7	A	B	15
8	B	B	18
9	B	B	20
10	B	B	21
11	B	B	23
12	B	C	2
13	B	C	4
14	B	C	5
15	B	C	7

Anode	CHIP	Connector	Pin Number
16	C	C	10
17	C	C	12
18	C	C	13
19	C	C	15
20	C	C	18
21	C	C	20
22	C	C	21
23	C	C	23
24	D	D	2
25	D	D	4
26	D	D	5
27	D	D	7
28	D	D	10
29	D	D	12
30	D	D	13
31	D	D	15

- Ground pin assignments:

Connector	Pin Number
A	2, 3, 6, 7, 10, 11, 14, 15, 18, 19, 22 and 23
B	1, 3, 6, 8, 9, 11, 14, 16, 17, 19, 22 and 24
C	1, 3, 6, 8, 9, 11, 14, 16, 17, 19, 22 and 24
D	1, 3, 6, 8, 9, 11, 14, 16, 17, 19, 22 and 24

- Unregulated power supply pin assignments:

Connector	Unregulated Supply	Pin Number
A	+ 6.0 Volts	13, 17 and 21
A	- 6.0 Volts	4, 8, 12, 16, 20 and 24
A	+ 3.0 Volts	1, 5 and 9

- Geographical address bits pin assignment:

ID Bit	Connector	Pin Number
S1	D	24
S2	D	23
S3	D	22
S4	D	21

b. Output connector pin assignment scheme:

Connector 1:

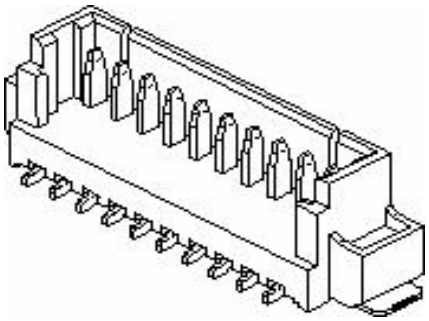
Signal	Pin Number	Signal	Pin Number
dE/dX 0	1	**R_dE/dX 0**	2
TR 0	3	**R_TR 0**	4
dE/dX 1	5	**R_dE/dX 1**	6
TR 1	7	**R_TR 1**	8
dE/dX 2	9	**R_dE/dX 2**	10
TR 2	11	**R_TR 2**	12
dE/dX 3	13	**R_dE/dX 3**	14
TR 3	15	**R_TR 3**	16
dE/dX 4	17	**R_dE/dX 4**	18
TR 4	19	**R_TR 4**	20
dE/dX 5	21	**R_dE/dX 5**	22
TR 5	23	**R_TR 5**	24
dE/dX 6	25	**R_dE/dX 6**	26
TR 6	27	**R_TR 6**	28
dE/dX 7	29	**R_dE/dX 7**	30
TR 7	31	**R_TR 7**	32
dE/dX 8	33	**R_dE/dX 8**	34
TR 8	35	**R_TR 8**	36
dE/dX 9	37	**R_dE/dX 9**	38
TR 9	39	**R_TR 9**	40
dE/dX 10	41	**R_dE/dX 10**	42
TR 10	43	**R_TR 10**	44
dE/dX 11	45	**R_dE/dX 11**	46
TR 11	47	**R_TR 11**	48
dE/dX 12	49	**R_dE/dX 12**	50
TR 12	51	**R_TR 12**	52
dE/dX 13	53	**R_dE/dX 13**	54
TR 13	55	**R_TR 13**	56
dE/dX 14	57	**R_dE/dX 14**	58
TR 14	59	**R_TR 14**	60
dE/dX 15	61	**R_dE/dX 15**	62
TR 15	63	**R_TR 15**	64
reserved	65	**reserved**	66
Rdbk_P	67	**Rdbk_N**	68
reserved	69	**reserved**	70
DATA_P	71	**DATA_N**	72
reserved	73	**reserved**	74
CLK_P	75	**CLK_N**	76
reserved	77	**reserved**	78
LD_P	79	**LD_N**	80

Connector 2:

Signal	Pin Number	Signal	Pin Number
dE/dX 16	1	**R_dE/dX 16**	2
TR 16	3	**R_TR 16**	4
dE/dX 17	5	**R_dE/dX 17**	6
TR 17	7	**R_TR 17**	8
dE/dX 18	9	**R_dE/dX 18**	10
TR 18	11	**R_TR 18**	12
dE/dX 19	13	**R_dE/dX 19**	14
TR 19	15	**R_TR 19**	16
dE/dX 20	17	**R_dE/dX 20**	18
TR 20	19	**R_TR 20**	20
dE/dX 21	21	**R_dE/dX 21**	22
TR 21	23	**R_TR 21**	24
dE/dX 22	25	**R_dE/dX 22**	26
TR 22	27	**R_TR 22**	28
dE/dX 23	29	**R_dE/dX 23**	30
TR 23	31	**R_TR 23**	32
dE/dX 24	33	**R_dE/dX 24**	34
TR 24	35	**R_TR 24**	36
dE/dX 25	37	**R_dE/dX 25**	38
TR 25	39	**R_TR 25**	40
dE/dX 26	41	**R_dE/dX 26**	42
TR 26	43	**R_TR 26**	44
dE/dX 27	45	**R_dE/dX 27**	46
TR 27	47	**R_TR 27**	48
dE/dX 28	49	**R_dE/dX 28**	50
TR 28	51	**R_TR 28**	52
dE/dX 29	53	**R_dE/dX 28**	54
TR 29	55	**R_TR 29**	56
dE/dX 30	57	**R_dE/dX 30**	58
TR 30	59	**R_TR 30**	60
dE/dX 31	61	**R_dE/dX 31**	62
TR 31	63	**R_TR 31**	64
reserved	65	**reserved**	66
reserved	67	**reserved**	68
Strobe_P	69	**Strobe_N**	70
reserved	71	**reserved**	72
S1_P	73	**S1_N**	74
S2_P	75	**S2_N**	76
S3_P	77	**S3_N**	78
S4_P	79	**S4_N**	80

c. Serial link diagnostic connector pin assignment:

Connector 3:



- The serial link diagnostic connector[viii] is an 8 contact wire to board header.

The pin assignment is as follows:

Signal	Pin Number
Rdbk_P	1
Rdbk_N	2
DATA_P	3
DATA_N	4
CLK_P	5
CLK_N	6
LD_P	7
LD_N	8

[i] AMP Z-PACK 2mm future bus Male connector. AMP Part number: 223513-1
[ii] In TEC, the PS board components are mounted on to the PC board such that they are facing the core of the detector.
[iii] Final Power consumption numbers will be made available when the design of Revision 2 of the Preamp shaper board is finalized. For detailed information refer to TEC-Preamp Shaper Power consumption document [Oct-07-1996].
[iv] Amphenol, 0.025" TWIST 'N' Flat planar cable 425 series, 80 conductors [40 twisted pairs]. Amphenol part number: 425-3006-080
[v] Amphenol 0.025" High Density cable mount IDC sockets. Amphenol Part number: 845-C080S-ALA55.
[vi] Amphenol 0.025" High Density board mounted straight IDC sockets. Amphenol Part number: 845-A080P-ALA55.
[vii] Same as endnote ii.
[viii] Molex 1.25mm wire to board header; Molex part number: 53398-0890

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